SUJAY DEB, PhD

Associate Professor and Head of Dept. of Electronics and Communication Engineering
Indraprastha Institute of Information Technology (IIIT) Delhi
Okhla, Phase-III, New Delhi-110020, INDIA
Office Phone: +91 11 2690 7452
Office Fax: +91 11 2690 7405
Email: sdeb@iiitd.ac.in
Web Page: http://www.iiitd.edu.in/~sdeb

Professional Experience

July 2018- present	Associate Professor, Indraprastha Institute of Information Technology (IIIT) Delhi
June 2012- June 2018	Assistant Professor, Indraprastha Institute of Information Technology (IIIT) Delhi
May 2011- August 2011	Summer Internship at Intel Labs, Hillsboro, OR, USA
August 2009 – May 2012	Research Assistant at the School of Electrical Engineering and Computer Science, Washington State University, Pullman, WA, USA
March 2005 – December 2007	Research Assistant in Computer Science and Engineering Dept., IIT Kharagpur, India

Education

Type	**Institute**	**Duration**	**Performance**
Graduate (**PhD** in Electrical and Computer Engineering)	Washington State University, Pullman, Washington, USA	2008-Feb'12	CGPA: 3.70/4
Graduate (**MS** in Telecommunication Engineering)	IIT Kharagpur, India	2005-2007	CGPA: 9.41/10
Under Graduate (**B.Tech**. in Electronics and Communication Engineering)	North Eastern Regional Institute of Science and Technology, India	2000-2004	CGPA: 4.31 / 5

Awards and Honors:

- Proposal got selected in Scheme for Promotion of Academic and Research Collaboration (**SPARC**) 2019.
- Selected as **Registration Chair of** IEEE International Conference on Embedded and VLSI Design (**VLSID**) 2019.
- **Publications** Chair of THE Ninth INTERNATIONAL GREEN and SUSTAINABLE COMPUTING CONFERENCE (IGSC) 2019 and 2018.
- **Publicity Chair** of IEEE International Conference on Embedded and VLSI Design (**VLSID**) 2017.
- **Track chair** of IEEE International Symposium on Nanoelectronic and Information Systems **(iNIS) 2016, 2017, 2018.**
- **Best paper award** in IEEE International Symposium on Nanoelectronic and Information Systems **(iNIS) 2017**.
- **Champion in VLSI Design Contest** 2017 held at IEEE International Conference on Embedded and VLSI Design conference (VLSID), Hyderabad.
- **Associate Editor** of IET Computers & Digital Techniques 2017.
- Invited to present our **startup idea in Nasscom Product Enclave** on 26-27 October 2016.
- Project on many-core coherence selected for **TCS PhD fellowship** in 2015.
- Winner of **India-US Grand Challenge**: Affordable Blood Pressure Measurement Technologies for Low-Resource Settings in India and the U.S. 2014.
- Innovation in Science Pursuit for Inspired Research **(INSPIRE) Faculty Award 2012**.
- **Outstanding PhD student Award** in Computer Engineering, School of EECS, WSU, 2011.
- **Travel Grant** for ISQED 2012 & SOCC 2010.
- **8th in 12th Class** Board Examination (Tripura, India), 2000 (top 0.05%).
- **2nd in 10th Class** Board Examination (Tripura, India), 1998 (top 0.01%).

Research Activities:

Research Interest Statement:

My research Interests are broadly in the areas of power and performance efficient and reliable Network-on-Chip (NoC) communication fabrics, Heterogeneous System Architectures (HSA), hardware for deep learning, low cost bio-sensors for preventive healthcare. More specifically, topics of interest include: intra and inter-chip wireless interconnection, efficient and reliable routing schemes, scalable coherence protocols for many-core systems, hardware support for on-chip

broadcast and multi-cast traffic, cache architectures for HSA, single chip bio potential acquisition system for preventive health-care. I also work on application of technology to healthcare, autonomous vehicles, mobile sensing etc.

Publication Citations
(Google Scholar as of 30 April, 2019)

	All	Since 2014
Citations	1376	1187
h-index	17	16
i10-index	23	23

Sponsored Projects

1. Title: Post-Silicon Debug Platform for Secure Systems
    a. Sponsoring Agency: SPARC
    b. PI:Sujay Deb
    c. Amount: Rs. 47,99,376
    d. Duration: 2 years (2019-2021)
2. Title: Cardio Watch: A cuff-less, low-cost BP monitoring solution
    a. Sponsoring Agency: DST
    b. PI:Sujay Deb
    c. Amount: Rs. 6,00,000
    d. Duration: 1 years (2019-2020)
3. Title: Emerging interconnects for future NoCs
    a. Sponsoring Agency: DST INSPIRE
    b. PI:Sujay Deb
    c. Amount: Rs. 35,00,000
    d. Duration: 5 years (2013-2018)
4. Title: A Low Cost and Easy to use Cuff-less Blood Pressure Measuring Device using Pulse Transit Time and Pre-ejection Period
    a. Sponsoring Agency: India-US Grand Challenge: Affordable Blood Pressure Measurement Technologies for Low-Resource Settings in India and the U.S.
    b. PI: Sujay Deb, Co-PI: Angshul Majumdar, Dr. Manoj K. Das (The INCLEN Trust)
    c. Amount: Rs. 40,94,000
    d. Duration: 3 years (2015-2018)
5. Title: Humansense
    a. Sponsoring Agency: ITRA
    b. Co-PI:Sujay Deb
    c. Amount: Rs. 1.24 Cr
    d. Duration: 3 years (2015-2018)
6. Title: Mobile-based Diagnosis of Sleep Apnea
    a. Sponsoring Agency: DST
    b. PI:Vinayak Naik, Co-PI: Sujay Deb, Sriram K

c. Amount: Rs. 55,43,239
d. Duration: 3 years (2015-2018)

Publications:

Book Chapters:

1. Partha Pratim Pande, Amlan Ganguly, **Sujay Deb** and Kevin Chang, Energy-Efficient Network-on-Chip Architectures for Multicore Systems, Handbook of Energy-Aware and Green Computing, Ishfaq Ahmad and Sanjay Ranka (Editors), Publisher: Chapman and Hall/CRC Press Taylor and Francis Group LLC.

Journals:

1. Sri Harsha Gade, M. Meraj Ahmde, **Sujay Deb** and Amlan Ganguly, "Energy Efficient Chip-to-Chip Wireless Interconnection for Heterogeneous Architectures", *ACM Transactions on Design Automation of Electronic Systems (**TODAES**)*, July 2019 (Accepted).
2. Sri Harsha Gade, Shobha Sundar Ram and **Sujay Deb**, "Millimeter wave wireless interconnects in deep submicron chips: Challenges and opportunities", *Integration, the VLSI Journal*, Vol. 64, Jan 2019, pp. 127-136.
3. Nishtha Wadhwa, Pydi Ganga Bahubalindruni, Kamal Chapagai, Joao Goes, Sujay Deb and Pedro Barquinha, "6th Order Differential Sallen-and-Key Switched Capacitor LPF using a-IGZO TFTs", *International Journal of Circuit Theory and Applications (IJCTA)***,** Vol. 47, Issue 1, Jan 2019, pp. 32-42.
4. Wazir Singh and Sujay Deb, "Biopotential Acquisition Unit For Energy Efficient Wearable Health Monitoring", *IET Cyber-Physical Systems: Theory & Applications*, vol. 3, Issue 2, June 2018, pp. 73-80.
5. Hemanta Kumar Mondal, Shri Harsha Gade, Shashwat Kaushik and **Sujay Deb**," Adaptive Multi-Voltage Scaling with Utilization Prediction for Energy-efficient Wireless NoC", IEEE Transactions on Sustainable Computing (**TSUSC**), Vol. 2, Issue:4, pp. 382-395, August 2017.
6. Hemanta Kumar Mondal, Sri Harsha Gade, Raghav Kishore, and **Sujay Deb**, "P2NoC: Power- and Performance-aware NoC Architectures for Sustainable Computing", Elsevier Journal of Sustainable Computing : Informatics and Systems, Vol. 16, pp. 25-37, December 2017.
7. Sri Harsha Gade, **Sujay Deb**, "HyWin: Hybrid Wireless NoC with Sandboxed Sub-networks for CPU/GPU Architectures", IEEE Transactions on Computers (**TC**), Vol. 66, Issue: 7, pp. 1145-1158, July 2017.
8. Wazir Singh, Ankita Shukla, **Sujay Deb** and Angshul Majumdar, "Energy Efficient EEG Acquisition and Reconstruction for a Wireless Body Area Network," Integration, the VLSI Journal, Vol. 58, pp. 295-302, June 2017.
9. Hemanta Kumar Mondal, Sri Harsha Gade, M S Shamim, **Sujay Deb**, and Amlan Ganguly, "Interference-Aware Wireless Network-on-Chip Architecture using Directional Antennas", IEEE Transactions on Multi-Scale Computing Systems (**TMSCS**), Vol. 3, Issue: 3,pp. 193-205,July-Sept 2017.

10. **Deb, S.**; Chang, K.; Xinmin Yu; Sah, S.P.; Cosic, M.; Ganguly, A.; Pande, P.P.; Belzer, B.; Deukhyoun Heo, "Design of an Energy-Efficient CMOS-Compatible NoC Architecture with Millimeter-Wave Wireless Interconnects," *Computers, IEEE Transactions on* (**TC**), vol.62, no.12, pp.2382,2396, Dec. 2013.
11. **Deb, S.**; Ganguly, A.; Pande, P.P.; Belzer, B.; Heo, D., "Wireless NoC as Interconnection Backbone for Multicore Chips: Promises and Challenges," *Emerging and Selected Topics in Circuits and Systems, IEEE Journal on* (**JETCAS**), vol.2, no.2, pp.228,239, June 2012.
12. Kevin Chang, **Sujay Deb**, Amlan Ganguly, Xinmin Yu, Suman Prasad Sah, Partha Pratim Pande, Benjamin Belzer, and Deukhyoun Heo. 2012. Performance evaluation and design trade-offs for wireless network-on-chip architectures. *J. Emerg. Technol. Comput. Syst.* (**JETC**) 8, 3, Article 23 (August 2012), 25 pages
13. Ganguly, A.; Chang, K.; **Deb, S.**; Pande, P.P.; Belzer, B.; Teuscher, C., "Scalable Hybrid Wireless Network-on-Chip Architectures for Multicore Systems," *Computers, IEEE Transactions on (**TC**)* , vol.60, no.10, pp.1485,1502, Oct. 2011.

Conferences:

1. Nishtha Wadhwa, Pydi Ganga Bahubalindruni, Sujay Deb, Pedro Barquinha, "Bootstrapping Circuit with IGZO TFTs for On-Chip Power Supply Generation", IEEE International Symposium on Circuits and Systems (ISCAS), Sapporo, Japan, 2019, pp. 1-5.
2. Sidhartha Sankar Rout, Kanad Basu and **Sujay Deb**, "Efficient Post-Silicon Validation of Network-on-Chip using Wireless Links", 32nd IEEE International Conference on VLSI Design (VLSID), New Delhi, India, 2019, pp. 371-376.
3. Soumya Jindal, Wazir Singh, Sujay Deb, "A Low-Cost Smart Vein Viewer System", IEEE International Symposium on Smart Electronic Systems (iSES)(Formerly iNiS), 2018, pp. 114-117.
4. Sri Harsha Gade, Sidhartha Sankar Rout, Ravi Kashyap, Sujay Deb, "Reliability Analysis of On-Chip Wireless Links for Many Core WNoCs", Conference on Design of Circuits and Integrated Systems (DCIS), 2018, pp. 1-6.
5. Mitali Sinha, Sidhartha Sankar Rout, Sri Harsha Gade, Sujay Deb, "Near Threshold Last Level Cache for Energy Efficient Embedded Applications", Ninth International Green and Sustainable Computing Conference (IGSC), 2018, pp. 1-6.
6. H. K. Mondal, R. C. Cataldo, C. Marcon, K. Martin, S. Deb and J-Ph. Diguet, "*Broadcast- And Power-aware Wireless NoC for Barrier Synchronization in Parallel Computing*", 31st IEEE Int. System-on-Chip Conference (**SOCC**), Washington DC, USA, Sep. 2018, pp. 1-6.
7. Sri Harsha Gade, Sidhartha Sankar Rout, Sujay Deb, "On-Chip Wireless Channel Propagation: Impact of Antenna Directionality and Placement on Channel Performance", *12th IEEE/ACM International Symposium on Networks-on-Chip (**NOCS**),* 2018, pp. 1-8.

8. Mitali Sinha, Harsha Gns, Wazir Singh and Sujay Deb, “Data-flow Aware CNN Accelerator with Hybrid Wireless Interconnection”, 29th Annual IEEE International Conference on Application-specific Systems, Architectures and Processors (**ASAP**),2018, pp. 1-4.
9. Nishtha Wadhwa, Pydi Bahubalindruni, and Sujay Deb, “A PVT Insensitive Low-power Differential Ring Oscillator”, 22nd International Symposium on VLSI Design and Test (**VDAT**), 2018, pp. 77-87.
10. Nishtha Wadhwa, Pydi Bahubalindruni, Sujay Deb and Pedro Barquinha, “A Comparitive Study of On-Chip Clock Generators Using a-IGZO TFTs for Flexible Electronic Systems”, IEEE International Flexible Electronics Technology Conference (IFETC), 2018, pp. 1-6.
11. Ankit Rehani, Sujay Deb, Pydi Ganga Bahubalindruni, Bhavin Odedara, and Srikanth Bojja, “A High-Efficient Current-Mode PWM DC-DC Buck Converter Using Dynamic Frequency Scaling”, IEEE International Symposium on VLSI (**ISVLSI**) 2018, pp. 464-469.
12. Sri Harsha Gade, Mitali Sinha, Sidhartha Sankar Rout, and Sujay Deb, “Enabling Reliable High Throughput On-Chip Wireless Communication for Many Core Architectures”, IEEE International Symposium on VLSI (**ISVLSI**) 2018, pp. 591-596.
13. Sri Harsha Gade, Hemanta Kumar Mondal, and Sujay Deb, “High Bandwidth Off-Chip Memory Access Through Hybrid Switching and Inter-Chip Wireless Links”, IEEE International Symposium on VLSI (**ISVLSI**) 2018, pp. 100-105.
14. Sri Harsha Gade, Sidhartha Sankar Rout, Mitali Sinha, Hemanta Kumar Mondal, Wazir Singh, and Sujay Deb, “A Utilization Aware Robust Channel Access Mechanism for Wireless NoCs“, IEEE International Symposium on Circuits and Systems (**ISCAS**)2018, pp. 1-5.
15. Sidhartha Sankar Rout, Hemanta Kumar Mondal, Rohan Juneja, Sri Harsha Gade and Sujay Deb, “Dynamic NoC Platfrom for Varied Application Needs”, accepted at The ***19th International Symposium on Quality Electronic Design (ISQED)*** 2018, pp. 232-237.
16. Shrestha Bansal, Hemanta Kumar Mondal, Sri Harsha Gade and Sujay Deb, “Energy Efficient NoC Router for High Throughput Applications in Many-core GPUs”, IEEE International Symposium on Nanoelectronic and Information Systems (**iNIS**) 2017, pp. 50-55. (**Won the Best Paper award**)
17. Sri Harsha Gade, Sakshi Garg and Sujay Deb, “OFDM based High Data Rate, Fading Resilient Transceiver for Wireless Networks-on-Chip”, in IEEE Computer Society Annual Symposium on VLSI (**ISVLSI**), 2017, pp. 483-488.
18. Shashwat Kaushik, Muni Agrawal, Hemanta Kumar Mondal, GNS Harsha and Sujay Deb, “Path Loss-Aware Adaptive Transmission Power Control Scheme for Energy-Efficient Wireless NoC” in 60th IEEE International Midwest Symposium on Circuits and Systems (**MWSCAS**), 2017, pp. 132-135.
19. Wazir Singh, Yathartha Gupta, Paritosh Jivani and Sujay Deb, “Energy Efficient Biopotential Acquisition Unit for Wearable Health Monitoring Applications”, **ISQED** 2017, pp. 337-341.
20. Hemanta Kumar Mondal, Shashwat Kaushik, Sri Harsha Gade, and Sujay Deb, “Energy-efficient Transceiver for Wireless NoC,” 30th International Conference on VLSI Design (**VLSID**), Hyderabad, January 2017, pp. 87-92.

21. Yatharth Gupta, Sujay Deb, Vikrant Singh, V N Srinivasan, Manish Sharma and Sabyasachi Das, “Pseudo-BIST: A Novel Technique for SAR-ADC Testing”, in 21st International Symposium on VLSI Design and Test (**VDAT** 2017), pp. 168-178.
22. Aartika Sethi, Sujay Deb, Prabhat Ranjan, Arghya Sardar, “Smart Mobility Solution with Multiple Input Output Interface”, in 39th Annual International Conference of the IEEE Engineering in Medicine and Biology Society (**EMBC**), 2017, pp. 3781-3784.
23. Suprateek Shukla, Ankit Rehani and Sujay Deb, “Enhancing Retention Voltage for SRAM”, in 21st International Symposium on VLSI Design and Test (**VDAT** 2017), pp. 406-413.
24. Pawan Sehgal, Akhilesh C Mishra, Rangarajan Ramanujam, Sujay Deb, “An Efficient Approach Targeting Broken Topological Clock Path for Master—Generated Clock Pair”, IEEE International Symposium on Nanoelectronic and Information Systems (**iNIS**), 2016, pp. 102-107.
25. Monika Jain, Sujay Deb, AV Subramanyam, “Face video based touchless blood pressure and heart rate estimation” IEEE 18th International Workshop on Multimedia Signal Processing (**MMSP**), 2016.
26. Monika Jain, Niranjan Kumar, Sujay Deb, “An affordable cuff-less blood pressure estimation solution” IEEE 38th Annual International Conference of the Engineering in Medicine and Biology Society (**EMBC**), 2016.
27. Sri Harsha Gade, Praveen Kumar and Sujay Deb, “A Pre-RTL Floorplanner Tool for Automated CMP Design Space Exploration with Thermal Awareness“, In Proceedings of IEEE 20th International Conference on VLSI Design and Test (**VDAT**), IIT Guwahati, India, May 2016.
28. Raghav Kishore, Hemanta Mondal and Sujay Deb, “Energy-efficient Reconfigurable Framework for Evaluating Hybrid NoCs“, In Proceedings of IEEE 20th International Conference on VLSI Design and Test (**VDAT**), IIT Guwahati, India, May 2016.
29. Pawan Sehgal and Sujay Deb , “An Effective and Efficient Algorithm to Analyse and Debug Clock Propagation Issues“, In Proceedings of IEEE 20th International Conference on VLSI Design and Test (**VDAT**), IIT Guwahati, India, May 2016.
30. M. Jain, N. Kumar and S. Deb, “A multi-signal acquisition system for preventive cardiology with cuff-less BP measurement capability“, 8th International Conference on Communication Systems and Networks (**COMSNETS**), Bangalore, pp. 1-6, 2016.
31. M. Jain, N. Kumar, S. Deb and A. Majumdar, “A sparse regression based approach for cuff-less blood pressure measurement“, IEEE International Conference on Acoustics, Speech and Signal Processing (**ICASSP**), Shanghai, pp. 789-793, 2016.
32. Hemanta Kumar Mondal, Sri Harsha Gade, Raghav Kishore, and Sujay Deb, “Adaptive Multi-Voltage Scaling in Wireless NoC for High-Performance Low Power Applications,” Design, Automation and Test in Europe (**DATE**), March 2016.
33. Hemanta Kumar Mondal, Sri Harsha Gade, Raghav Kishore, Shashwat Kaushik and Sujay Deb, “Power Efficient Router Architecture for Wireless Network-on-Chip,” 17th International Symposium on Quality Electronic Design (**ISQED**), March 2016.

34. Pallavi Das, Jitendra Yadav and Sujay Deb,"Mixed Mode Simulation and Verification of SSCG PLL through Real Value Modeling" 29th IEEE International Conference on VLSI Design (**VLSID**), January 2016.
35. Tanya Shreedhar and Sujay Deb, "Hierarchical Cluster-based NoC design using Wireless Interconnects for Coherence Support" 29th IEEE International Conference on VLSI Design (**VLSID**), January 2016.
36. Wazir Singh and Sujay Deb, "Energy Efficient and Congestion-Aware Router Design for NoCs," 29th IEEE International Conference on VLSI Design (**VLSID**), pp. 81-85, January 2016.
37. Wazir Singh and Sujay Deb, "Energy Efficient Analog-to-Information Converter for Biopotential Acquisition Systems," IEEE International Symposium on Nanoelectronic and Information Systems (**iNIS**), pp. 141-145, December 2015.
38. Hemanta Kumar Mondal, Sri Harsha Gade, Raghav Kishore and Sujay Deb, "Power and Performance-Aware Fine-Grained Reconfigurable Router Architecture for NoC," International Green and Sustainable Computing Conference **(IGSC),** ***December 2015.***
39. Gade, Sri Harsha, and Sujay Deb. "Achievable Performance Enhancements with mm-Wave Wireless Interconnects in NoC." *Proceedings of the 9th International Symposium on Networks-on-Chip (**NOCS**)*. ACM, 2015.
40. Vijender Kumar Sharma, Jai Narayan Tripathi, Rajkumar Nagpal, Sujay Deb, Rakesh Malik," Estimation of Inter Symbol Interference using Clock Pattern,"2015 16th International Conference on Electronic Packaging Technology (**ICEPT**), pp. 1409-1412, August 2015
41. Malhotra, Rahul; Deb, Sujay; Carlucci, Fabio,"A novel approach to reusable time-economized STIL based pattern development," 2015 19th International Symposium on VLSI Design and Test (**VDAT**), pp. 1-5, June 2015
42. Kaur, Ramandeep; Malhotra, Rahul; Deb, Sujay, "MAC based FIR filter: A novel approach for low-power real-time de-noising of ECG signals," 2015 19th International Symposium on VLSI Design and Test (**VDAT**), pp. 1-5, June 2015
43. Singh, Namrata; Deb, Sujay, "Analysis and design guidelines for customized logic families in CMOS, " 2015 19th International Symposium on VLSI Design and Test (**VDAT**), pp. 1-2, June 2015
44. Gade, Sri Harsha; Mondal, Hemanta Kumar; Deb, Sujay, "A Hardware and Thermal Analysis of DVFS in a Multi-core System with Hybrid WNoC Architecture," *VLSI Design (**VLSID**), 2015 28th International Conference on* , vol., no., pp.117,122, 3-7 Jan. 2015
45. Deb, S.; Mondal, H., "Wireless network-on-chip: a new era in multi-core chip design," *Rapid System Prototyping (**RSP**), 2014 25th IEEE International Symposium on* , vol., no., pp.59,64, 16-17 Oct. 2014 (***Invited Paper***)
46. Mondal, H.K.; Deb, S., "An energy efficient wireless Network-on-Chip using power-gated transceivers," *System-on-Chip Conference (**SOCC**), 2014 27th IEEE International* , vol., no., pp.243,248, 2-5 Sept. 2014

47. Singh, W.; Shukla, A.; Deb, S.; Majumdar, A., "Energy efficient acquisition and reconstruction of EEG signals," *Engineering in Medicine and Biology Society (**EMBC**), 2014 36th Annual International Conference of the IEEE* , vol., no., pp.1274,1277, 26-30 Aug. 2014
48. Mondal, H.K.; Sri Harsha, G.N.; Deb, S., "An Efficient Hardware Implementation of DVFS in Multi-core System with Wireless Network-on-Chip," *VLSI (**ISVLSI**), 2014 IEEE Computer Society Annual Symposium on* , vol., no., pp.184,189, 9-11 July 2014
49. Samaiyar, A.; Ram, S.S.; Deb, S., "Millimeter-wave planar log periodic antenna for on-chip wireless interconnects," *Antennas and Propagation (**EuCAP**), 2014 8th European Conference on* , vol., no., pp.1007,1009, 6-11 April 2014
50. Md Shahriar Shamim, Naseef Mansoor, Aman Samaiyar, Amlan Ganguly, Sujay Deb, and Shobha Sunndar Ram. 2014. Energy-efficient wireless network-on-chip architecture with log-periodic on-chip antennas. In *Proceedings of the 24th edition of the great lakes symposium on VLSI* (**GLSVLSI**). ACM, New York, NY, USA, 85-86
51. Kanva, A.K.; Sharma, C.J.; Deb, S., "Determination of SpO2 and heart-rate using smartphone camera," *Control, Instrumentation, Energy and Communication (**CIEC**), 2014 International Conference on* , vol., no., pp.237,241, Jan. 31 2014-Feb. 2 2014
52. Mondal, H.K.; Deb, S., "Energy efficient on-chip wireless interconnects with sleepy transceivers," *Design and Test Symposium (**IDT**), 2013 8th International* , vol., no., pp.1,6, 16-18 Dec. 2013
53. Wettin, P.; Pande, P.P.; Deukhyoun Heo; Belzer, B.; Deb, S.; Ganguly, A., "Design space exploration for reliable mm-wave wireless NoC architectures," *Application-Specific Systems, Architectures and Processors (**ASAP**), 2013 IEEE 24th International Conference on* , vol., no., pp.79,82, 5-7 June 2013
54. Das, S.; Srikrishna, S.; Shukla, A.; Harsha, G.; Deb, S., "A low-cost non-intrusive appliance load monitoring system," *Advance Computing Conference (**IACC**), 2013 IEEE 3rd International* , vol., no., pp.1641,1644, 22-23 Feb. 2013
55. Deb, S.; Deb, S., "Designing an intelligent blink analyzer tool for effective human computer interaction through eye," *Intelligent Human Computer Interaction (**IHCI**), 2012 4th International Conference on* , vol., no., pp.1,5, 27-29 Dec. 2012
56. Sujay Deb, Kevin Chang, Miralem Cosic, Amlan Ganguly, Partha P. Pande, Deukhyoun Heo, and Benjamin Belzer. 2012. CMOS compatible many-core noc architectures with multi-channel millimeter-wave wireless links. In *Proceedings of the great lakes symposium on VLSI* (**GLSVLSI**). ACM, New York, NY, USA, 165-170
57. Deb, S.; Chang, K.; Ganguly, A.; Xinmin Yu; Teuscher, C.; Pande, P.; Heo, D.; Belzer, B., "Design of an efficient NoC architecture using millimeter-wave wireless links,"*Quality Electronic Design (**ISQED**), 2012 13th International Symposium on* , vol., no., pp.165,172, 19-21 March 2012
58. Xinmin Yu; Sah, S.P.; Deb, S.; Pande, P.P.; Belzer, B.; Deukhyoun Heo, "A wideband body-enabled millimeter-wave transceiver for wireless Network-on-Chip," *Circuits and Systems (**MWSCAS**), 2011 IEEE 54th International Midwest Symposium on* , vol., no., pp.1,4, 7-10 Aug. 2011

59. Deb, S.; Chang, K.; Ganguly, A.; Pande, P., "Comparative performance evaluation of wireless and optical NoC architectures," *SOC Conference (**SOCC**), 2010 IEEE International* , vol., no., pp.487,492, 27-29 Sept. 2010
60. Deb, S.; Ganguly, A.; Chang, K.; Pande, P.; Beizer, B.; Heo, D., "Enhancing performance of network-on-chip architectures with millimeter-wave wireless interconnects," *Application-specific Systems Architectures and Processors (**ASAP**), 2010 21st IEEE International Conference on* , vol., no., pp.73,80, 7-9 July 2010
61. Sujay Deb; Nanda, C.; Goswami, D.; Mukhopadhyay, J.; Chakrabarti, S., "Cuff-Less Estimation of Blood Pressure Using Pulse Transit Time and Pre-ejection Period,"*Convergence Information Technology, 2007. International Conference on* , vol., no., pp.941,944, 21-23 Nov. 2007
62. Sujay Deb, D. Goswami, J. Mukhopadhyay, S. Chakrabarti, "A Proposition for Low Cost Preventive Cardiology for Rural Health Care System",presented in eHealth Asia Conference 2007,Malaysia
63. Deb, S.; Deb, S., "Single Key Omni directional Pointing and command System (SKOPS) -a smart on-screen navigational tool for physically disabled persons," *e-Health Networking, Application and Services, 2007 9th International Conference on* , vol., no., pp.197,201, 19-22 June 2007
64. Anant Kumar Jain, Sujay Deb, D. Goswami, Alok Barua, J. Mukhopadhyay and S. Chakrabarti, "Determination of SpO_2 by Spectral Analysis of Data from a Low Cost Pulse Oximeter", Proceedings of the Indian Conference on Medical Informatics and Telemedicine (**ICMIT**), IIT Kharagpur 2006, pp. 10-13.
65. Suman Deb, Sujay Deb, "Text to Indian Sign Language Generation Engine (TILE): A Self Training and Communication Tool for Hearing Impaired Persons", Proceedings of the Indian Conference on Medical Informatics and Telemedicine (**ICMIT**), IIT Kharagpur 2006, pp. 14-16.

Conference Tutorials:

1. Sujay Deb, "Communication Infrastructure for Future Exascale Processors" Half day tutorial at IEEE VLSI Design Conference (VLSID), Hyderabad, India, Jan 2017.
2. Sujay Deb, "Energy efficient network on chip design for future many-core processors", Half day tutorial at IEEE VLSI Design and Test Conference (VDAT), Guwahati, India, May 2016.

Workshop/ Demo Papers:

1. Niranjan Kumar, Amogh Agrawal, Sujay Deb," Cuffless BP Measurement Using a Correlation Study of Pulse Transient Time and Heart Rate" in ICACCI 2014.
2. Renduchinthala Anusha, Surat Swarup Devulapalli, Akhilesh Chandra Mishra, Sujay Deb," An efficient approach to smoothen UPF management at SoC level", Design and Verification Conference and Exhibition (DVCon), India, 2016.

3. Jain, M., Deb, S. & Majumdar, M., “Robust Blood Pressure Prediction Using Learned Dictionaries”, 38th Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC).
4. Jain, M., Deb, S. & Majumdar, M., "A Cuff-less Blood Pressure Monitoring Solution", 38th Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC).
5. Sujay Deb, Niranjan Kumar, Rahul Gupta, Manoj Gulati, “CardioWatch: An Initiative Towards Affordable Preventive Cardiovascular Healthcare” Presented in COMSNET 2014.

Invited Talks:

1. “HyWin: A High-Performance Interconnection Platform for Heterogeneous System Architectures”, Rochester Institute of Technology, Department of Computer Engineering, August 9, 2017.
2. “CardioWatch:A Comprehensive, Low-cost BP Monitoring Solution”, in Nasscom Product Enclave on 26-27 October 2016.
3. Invited lecture at STTP on VLSI and Embedded System Design, at Nirma University on May 24, 2016
4. Invited lecture at Faculty Development program at Jaypee Institute of Information Technology, Noida, on July 18, 2016.
5. Invited lecture at Tripura Institute of Technology, Tripura on Current research trends in VLSI on 31st October 2016.
6. Invited expert lecture in the workshop on circuits and system design challenges for IoT at Aligarh Muslim University, Aligarh on February 18, 2017.
7. “Promises & Challenges of Wireless Network-on-Chip”, HiPC 2014.
8. “Wireless Network-on-Chip: A New Era in Multi-Core Chip Design”, Embedded Systems Week 2014.
9. Invited talk at NIT Silchar on ‘Wireless Network on Chip’ on February 2014.
10. Invited talk at NERIST on ‘VLSI Design: The Road Ahead’ on July 2013.

Patents:

Patent # 1:

a) Application No. 201611028804
b) Title: Cuff-less Blood Pressure Estimation Solution Using Electrocardiogram and Photoplethysmogram
c) Inventors: Monika Jain, A V Subramanyam, Sujay Deb and Angshul Majumdar.
d) Status: Filed/ Granted: Filed
e) Date for filing/ Granted: 24/08/2016
f) Publication date: 30/03/2018

Patent # 2:

a) Application No. 201711028803

b) Title: Smartphone Based Health Monitoring Using the Inbuilt Camera
c) Inventors: Monika Jain, Sujay Deb and Angshul Majumdar.
d) Status: Filed/ Granted: Filed
e) Date for filing/ Granted: 24/08/2016
f) Publication date: 30/03/2018

Patent # 3:

a) Application No. 201911006527
b) Title: Method and System for Post Silicon Validation
c) Inventors: Sidhartha Sankar Rout and Sujay Deb
d) Status: Filed/ Granted: Filed
e) Date for filing/ Granted: 19/02/2019

Educational Activities

Graduated PhD Students:

1. Hemanta Kumar Mondal (Jan 2013- August 2017), Currently working as Assistant Professor at NIT Durgapur, earlier worked as Assistant Professor at IIIT Guwahati, before that he was doing postdoc at CNRS Lab-STICC, University of Southern Brittany in Lorient, France.

   Topic: Power- and Performance-aware Interconnection Architecture for Many-core Systems

Current PhD Students:

1. Wazir Singh (May 2014- present)
2. GNS Harsha (Aug 2015- present)
3. Mitali Sinha (May 2017- present)
4. Sidhartha Sankar Rout (July 2017- present)

PhD students Co-advised by me:

5. Rakhi Hemani
6. Nishtha Wadhwa
7. Bhawna Tiwari
8. Belal Iqbal

Master Thesis students Graduated:

1. Sri Harsha Gade (MTech 2014, Title: An On-Chip Wireless Interconnect Based DVFS Implementation for future CMPs), Currently: PhD candidate at IIITD
2. Sidhartha Sankar Rout(MTech 2014, Title: Reliability Aware Intelligent Memory Management (RAIMM)), Currently: PhD candidate at IIITD
3. Vijender Sharma (MTech 2014, Title: Analysis and Estimation of Jitter Sub-Components) , Currently: PhD candidate at IIT Mandi
4. Pranay Samanta (MTech 2014, Title: UVM based STBUS Verification IP for verifying SoC), Currently: Intel, Bengaluru
5. Aditi Sharma (MTech 2015, Title: Smart and Efficient Multi-scenario SoC Timing Closure and ECO Generator), Currently: ST Microelectronics, Noida

6. Rahul Malhotra (MTech 2015, Title: A novel approach to Reusable Time-economized STIL based pattern development), Currently: ST Microelectronics, Noida
7. Raghav Madan (MTech 2015, Title: Development and enhancement of verification environment for complex designs), Currently: ST Microelectronics, Noida
8. Nidhi Chandoke (MTech 2015, Title: A SystemC TLM based Power Estimation Methodology to Enable Power Aware SoC Design), Currently: ST Microelectronics, Noida
9. Pallavi Das (MTech 2015, Title: Verification of Analog and Mixed signal IP through Real Value Modelling), Currently: Synopsys, Bengaluru
10. Raghav Kishore (MTech 2016, Title: Evaluation Framework for Technology Agnostic Hybrid NoC Architecture) Currently: AMD, Bengaluru
11. Antara Ganguly (MTech 2016, Title: Hardware support for broadcast and multicast traffic in future many core chips), Currently: Joined PhD at IIT Bombay
12. Pawan Sehgal (MTech 2016, Title: An Effective and Efficient Algorithm to Analyse and Debug Clock Propagation Issues), Currently: NXP, Noida
13. R Anusha (MTech 2016, Title: An Efficient Approach to Smoothen SoC's UPF Management) , Currently: Qualcomm, Bengaluru
14. Ankit Rehani (MTech 2018, Title: A High-Efficient Current-Mode PWM DC-DC Buck Converter Using Dynamic Frequency Scaling), Currently: Sandisk, Bengaluru
15. Suprateek Shukla (MTech 2018, Title: Low Swing NAND I/O Transmitter), Currently: Sandisk, Bengaluru

MTech Scholarly Papers / Capstone project completed

1. Yatharth Gupta (MTech 2017), Title: Pseudo-BIST: A Novel Technique for SAR-ADC Testing (published in VDAT 2017)
2. Aartika Sethi (MTech 2017), Title: Assistive technology for wheelchair based patients (published in EMBC 2017)
3. Chayan Pathak (MTech 2017), Title: Emerging communication infrastructure for intra and inter chip wireless communications
4. Ashwani (MTech 2014), Title: Energy Efficient Techniques For NoC
5. Rishabh Gupta (MTech 2013), Title: Low Power SoC Design strategies
6. Sakshi Narula (MTech 2013), Title: On-Chip Antennas for enabling intra-chip wireless communications
7. Kumar Abhishek (MTech 2012), Title: Power Efficient Switch Design for NoC Applications

PG Research/Independent Study or Independent Project completed:

1. Arjun Singh (Monsoon 2017), Title: Low-Voltage Low-Frequency Clock Generator
2. Akhil James (Summer 2017), Title: HSA coherence issues
3. Muni Agrawal (Summer 2017), Title: Variable gain PA design
4. Ankush Mamgain (Summer 2017), Title: Near Threshold circuits for memory design
5. Ishaind Gupta (Summer 2017), Title: Quality of Service, Reliability and Aging analysis of On-Chip Interconnects
6. Sadiq Husain (Summer 2017), Title: Band gap reference circuit

7. Mranal Kulshreshtha (Summer 2017), Title: On-Chip Communication Energy Reduction Through Reliability Aware Adaptive Voltage Swing Scaling
8. Sajal Khanna (Summer 2017), Title: Design and Implementation of power gated wireless interface access protocol
9. Soni Chintan Jayendrabhai (Summer 2017), Title: Techniques for Reducing the Latency in Multicore Processor Architecture
10. Abhinav Sharma (Summer 2017), Title: Power reduction in SAR Logic using Clock Gating technique
11. Shreshtha Bansal (Summer 2016), Title: Energy Efficient NoC Router for High Throughput Applications in Many-core GPUs (**iNIS 2017 best paper** winner)
12. Tanya Shreedhar (Summer 2015), Title: Hierarchical Cluster based NoC design using Wireless Interconnects for Coherence Support
13. Sidhartha Sankar Rout (Winter 2014), Title: Survey on open source NoC simulators

BTPs completed:

1. Rohan Juneja (Winter 2017- Monsoon 2017), Title: Memory architectures for future many-core processors
2. Aishwarya Raj (Winter 2017), Title: OFDM based on-chip wireless interconnects
3. Mukul Gupta (2012 ECE BTech student, IIIT D, with AMD) (Nominated for best BTP) Title: Analyzing IO subsystem performance for AMD and Intel APUs using IOMeter benchmark

Current BTech Project students:

1. Kaustubh Singh
2. Anukriti Yadv
3. Navneet Anand Sah

UG Research/Independent Study or Independent Project completed:

1. Shagun Kapur (Monsoon 2017), Title: OpenBCI based health monitoring system
2. Varshita Gupta (Monsoon 2017), Title: OpenBCI based health monitoring system
3. Deepanshu Gehlot (Winter 2017), Title: Mini Weather station design
4. Apurba Mondal (Winter 2017),Title: Vein assist: a tool to locate vein easily
5. Akash Aggarwal (Monsoon 2016), Title: Development of an integrated floor planning tool for many-core processors (**Won VLSI Design Contest 2017**)
6. Lakshit Tyagi (Monsoon 2016), Title: Development of an integrated floor planning tool for many-core processors (**Won VLSI Design Contest 2017**)
7. Ankit Girdhar (Monsoon 2016), Title: Memory architecture for future many-core architectures
8. Diljyot Singh Jaura (Monsoon 2016), Title: On-chip memories for futures many-core processors
9. Varun Kumar (Monsoon 2016), Title: On-chip memories for futures many-core processors
10. Rohan Juneja (Winter 2016), Title: Cache coherence issues in many-core processors
11. Abhinav Aggarwal (Monsoon 2015), Title: HR calculation from Smartphone Camera
12. Ankush Jolly (Monsoon 2015), Title: Developing compact wearable Bio-Medical Sensors for a continuous health monitoring

13. Akshay Punhani (Winter 2015), Title: Extraction of Diagnostic Features from simultaneously recorded physiological signals
14. Pulkit Kumar Gupta (Winter 2015), Title: Extraction of Diagnostic Features from simultaneously recorded physiological signals
15. Raghav Sehgal (Monsoon 2014) Title: Design of a smart phone based Phonocardiogram

BTech Interns (outside IIIT Delhi):

1. Avneendra Kumar Kanva (NSIT)
2. Chandan Jyoti Sharma (NSIT)
3. Aman Samaiyar (DTU)
4. Amogh Agrawal (IIT Ropar)
5. Jitesh Gupta (NSIT)
6. Jaidev Singh Chadha (DTU)
7. Simarpreet Singh Chawla (DTU)
8. Snigdha Kamal (DTU)
9. Satya Prakash (IIT Guwahati)
10. Adithya S P (VIT)
11. Ravi Kashyap (JIIT)
12. Twinkle Verma (JIIT)
13. Pranav Gulati (DTU)
14. Siddhartha Jain (BITS Pilani)
15. Guided 20 interns selected through **Summer Research Fellowship Programme (SRFP)** sponsored by the National Science Academy.

Research Associates:

1. Monika Jain (Currently doing PhD at IIIT Delhi)
2. Wazir Singh (Currently doing PhD in our group)
3. Niranjan Kumar (Currently in industry)
4. Ripudaman Khattar (Currently pursuing higher studies in USA)
5. Mitali Sinha (Currently doing PhD in our group)
6. Sugandha Bajaj
7. Mukul Gupta
8. Juhi Faridi

Professional and Institute Service

Service to Profession:

1. **Associate Editor** of IET Computers & Digital Techniques (From 2017- present).

2. **Publicity Chair** of IEEE International Conference on Embedded and VLSI Design (**VLSID**) 2017.

3. Selected as **Registration Chair of** IEEE International Conference on Embedded and VLSI Design (**VLSID**) 2019.

4. **Publications Chair** of THE Ninth INTERNATIONAL GREEN and SUSTAINABLE COMPUTING CONFERENCE (**IGSC**) 2018.

5. **Track chair** of IEEE International Symposium on Nanoelectronic and Information Systems **(iNIS) 2016 & 2017.**

6. We delivered a half-day **tutorial** at IEEE International Conference on Embedded and VLSI Design conference (**VLSID 2017**), Title: Communication Infrastructure for Future Exascale Processors.

7. Mini-symposia on BP estimation techniques was delivered at 39th Annual International Conference of the IEEE Engineering in Medicine and Biology Society (**EMBC**), 2017.
8. We delivered a very well attended tutorial on "Energy Efficient NoC Design for Future Many-core Processors" on 24th May 2016, at IEEE International Symposium on VLSI Design and Test (**VDT 2016**). Link: http://www.iitg.ernet.in/vdat2016/Tutorial.php
9. Our **Mini-symposia proposal on Cuff-less BP was accepted** at 38th Annual International Conference of the IEEE Engineering in Medicine and Biology Society (**EMBC**), Florida 2016.
10. Organized a one day **workshop on Network on Chip** on 29th March, 2015 at IIIT Delhi.

11. **TPC** member of VLSI Design Conference 2018, VLSID 2016, VLSID 2015, VLSID 2014, VDAT 2016, NetHealth 2016, GLSVLSI 2018, iNIS 2017, iNIS 2016, iNIS 2015.

12. Reviewer of TVLSI, TC, TCAD, TODAES, Access, TMSCS, JETC, SUSCOM, VLSI Design Conference, IGSC, GLSVLSI, VDAT, iNIS etc.

13. Panelist in a **panel discussion** on "Advances in MedTech and relevance to India" in **NetHealth Workshop** on 9th January 2016.

14. **Session chairs** at VLSID 2017, VDAT 2016, IGSC 2015.

Service to Institute:

1. Head of Dept. of ECE (since Jan 2018)

2. MTech Coordinator for VLSI & ES(2014-2016)

3. TA allocation committee (2016)

4. UG co-ordinator for ECE Dept. (2017)

5. Community work co-ordinator (2012-2014)

6. ESYA 2012 & 2013

External examiner:

1. PhD Students:

    a. Dr. Venkata Kalyan Tavva, IIT Madras, June 2015.

    b. Dr. Manoj Kumar, MNIT Jaipur, December 2016.

c. Dr. Rimpy, MNIT Jaipur, September 2015.

2. MTech Students:

a. MTech : 3 students IIT Delhi CSE. June 2013

b. MTech : 5 students IIT Delhi CSE. June 2014

c. MTech : 8 students SNU, ECE, May 2014

d. MTech : 4 students IIT Delhi CSE. June 2015

e. MTech : 3 students IIT Delhi CSE. June 2016

f. MTech : 4 students IIT Delhi CSE. June 2017

g. MTech: 8 students IIT Delhi CSE. June 2018

h. MTech: 3 students IIT Delhi CSE, April 2019